Figure 1

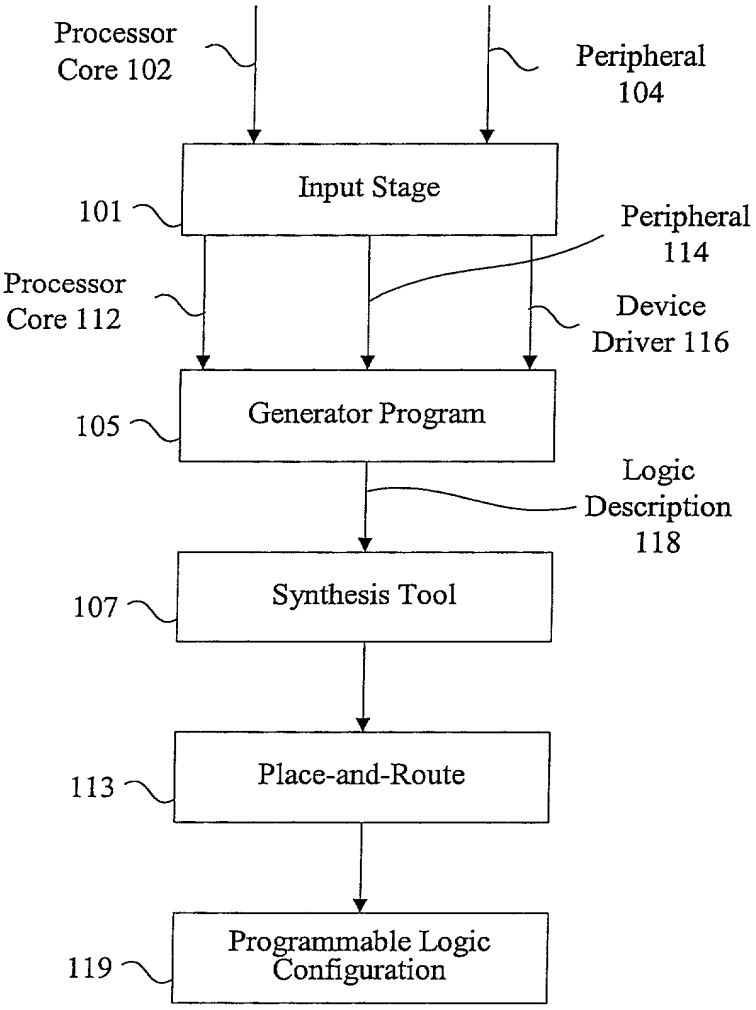

Processor Core 102
Peripheral 104
Input Stage
101
Peripheral 114
Processor Core 112
Device Driver 116
Generator Program
105
Logic Description 118
Synthesis Tool
107
Place-and-Route
113
Programmable Logic Configuration
119

Figure 2

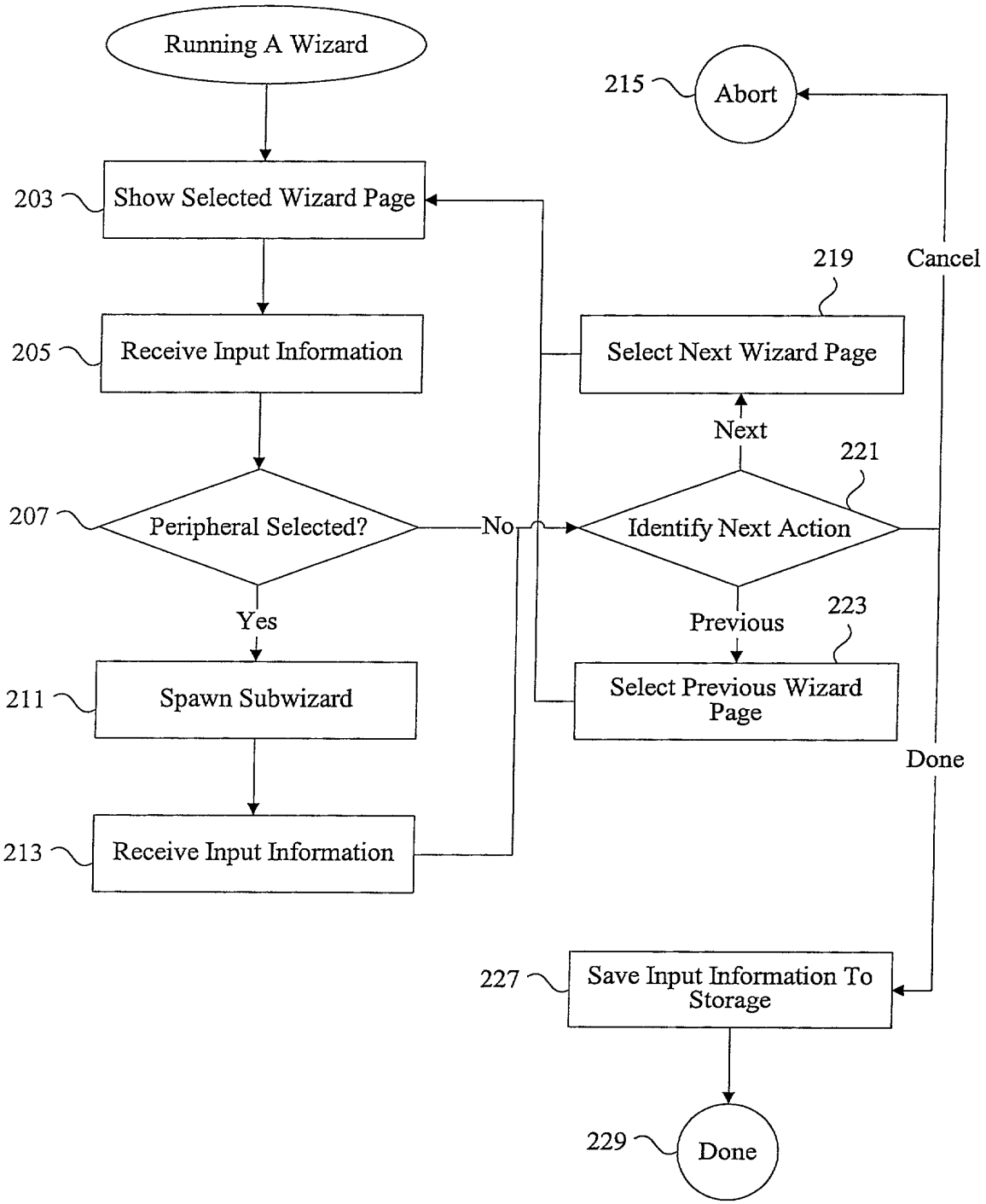

Running A Wizard
215
Abort
203
Show Selected Wizard Page
219
Cancel
205
Receive Input Information
Select Next Wizard Page
Next
221
207
Peripheral Selected?
No
Identify Next Action
Yes
Previous
223
211
Spawn Subwizard
Select Previous Wizard Page
Done
213
Receive Input Information
227
Save Input Information To Storage
229
Done

FIGURE 3A

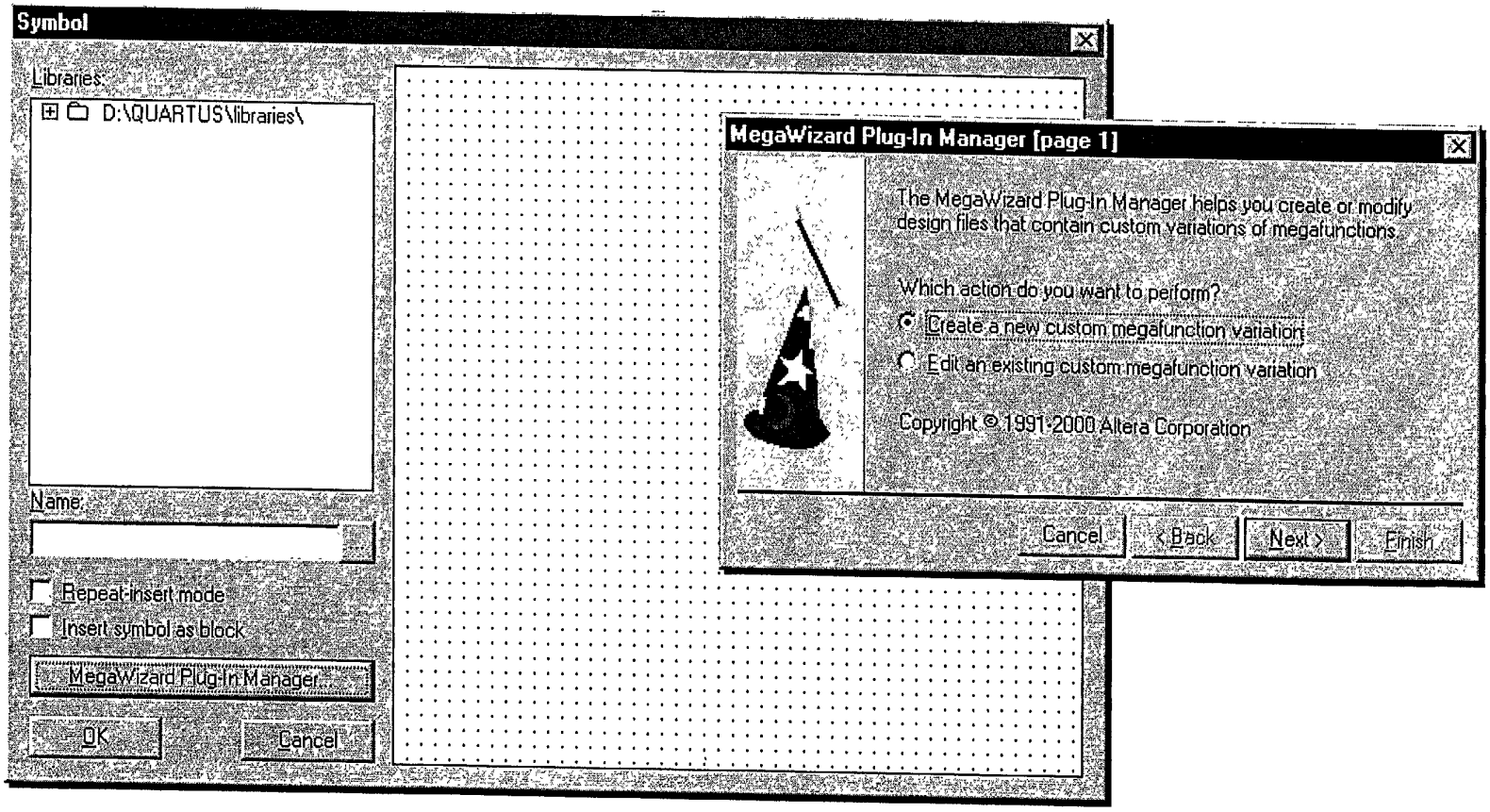

Symbol
Libraries:
D:\QUARTUS\libraries\
Name:
Repeat-insert mode
Insert symbol as block
MegaWizard Plug-In Manager...
OK
Cancel
MegaWizard Plug-In Manager [page 1]
The MegaWizard Plug-In Manager helps you create or modify design files that contain custom variations of megafunctions.
Which action do you want to perform?
Create a new custom megafunction variation
Edit an existing custom megafunction variation
Copyright © 1991-2000 Altera Corporation
Cancel
< Back
Next >
Finish

FIGURE 3B

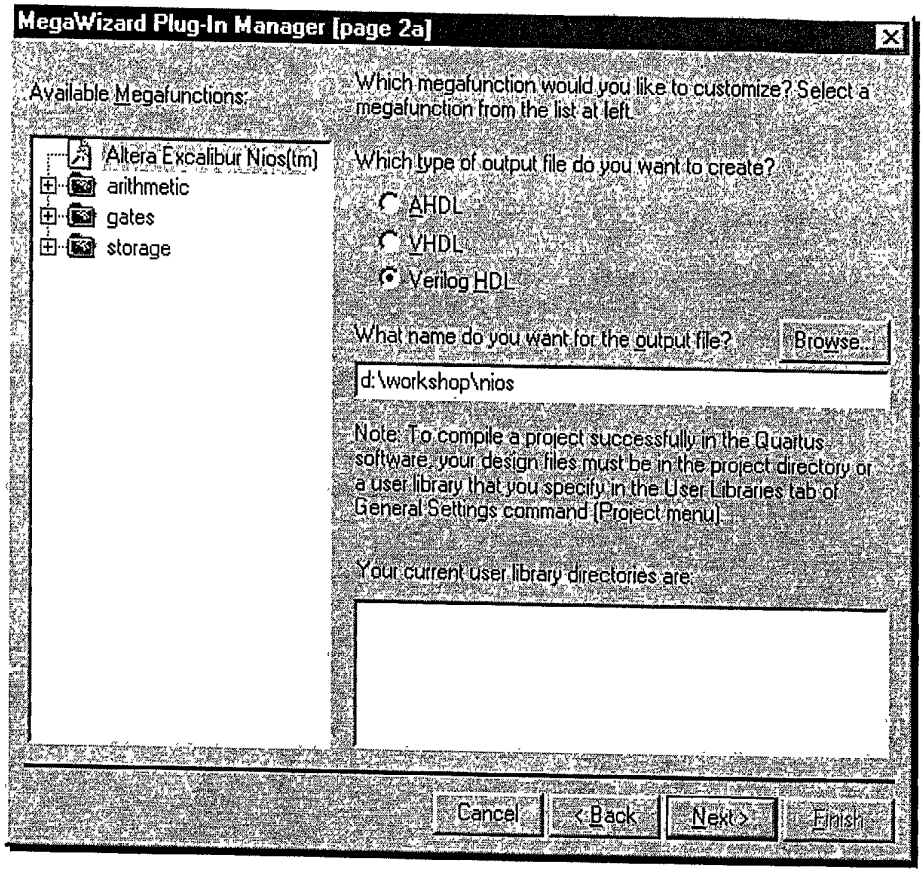


FIGURE 3C

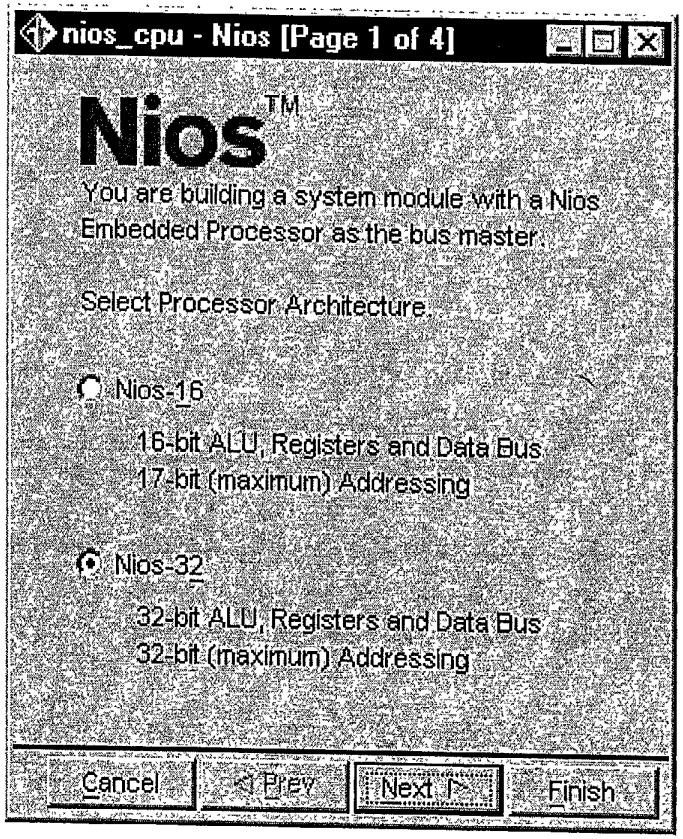

nios_cpu - Nios [Page 1 of 4]
Nios™
You are building a system module with a Nios Embedded Processor as the bus master.
Select Processor Architecture
Nios-16
16-bit ALU, Registers and Data Bus
17-bit (maximum) Addressing
Nios-32
32-bit ALU, Registers and Data Bus
32-bit (maximum) Addressing
Cancel
< Prev
Next >
Finish

FIGURE 3D

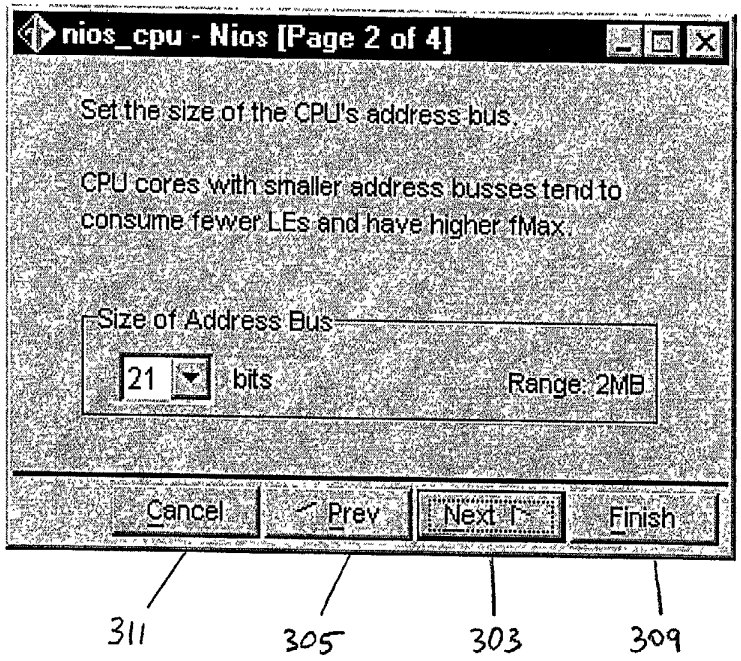

nios_cpu - Nios [Page 2 of 4]
Set the size of the CPU's address bus.
CPU cores with smaller address busses tend to consume fewer LEs and have higher fMax.
Size of Address Bus
21
bits
Range: 2MB
Cancel
< Prev
Next >
Finish
311
305
303
309

FIGURE 3E

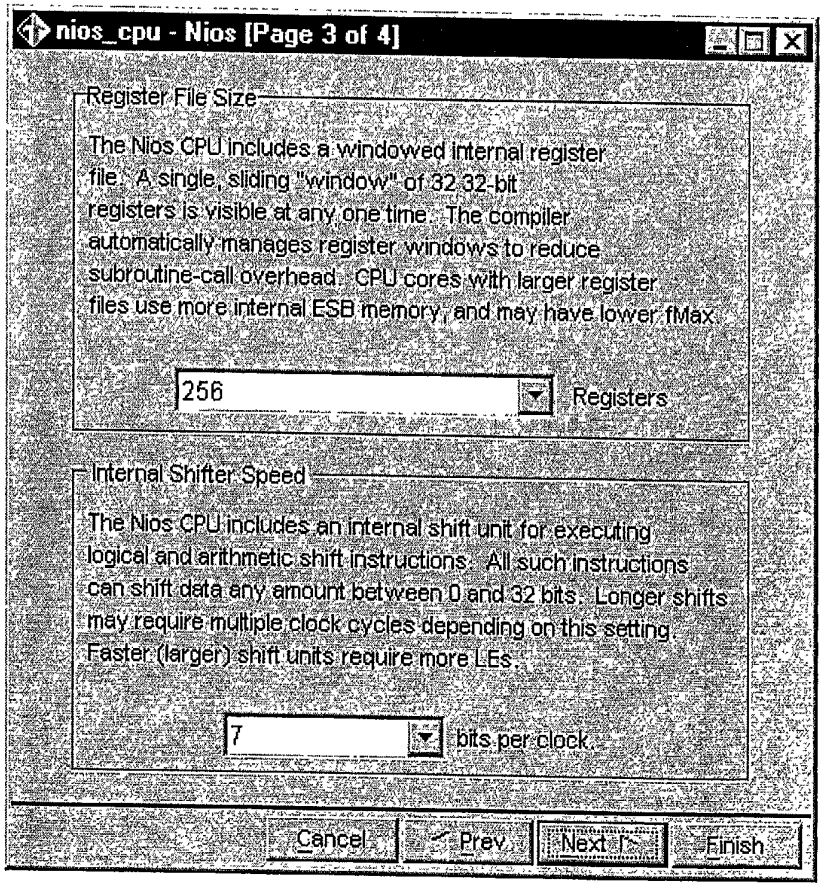

nios_cpu - Nios [Page 3 of 4]
Register File Size
The Nios CPU includes a windowed internal register file. A single, sliding "window" of 32 32-bit registers is visible at any one time. The compiler automatically manages register windows to reduce subroutine-call overhead. CPU cores with larger register files use more internal ESB memory, and may have lower fMax.
256
Registers
Internal Shifter Speed
The Nios CPU includes an internal shift unit for executing logical and arithmetic shift instructions. All such instructions can shift data any amount between 0 and 32 bits. Longer shifts may require multiple clock cycles depending on this setting. Faster (larger) shift units require more LEs.
1
bits per clock
Cancel
< Prev
Next >
Finish

FIGURE 3F

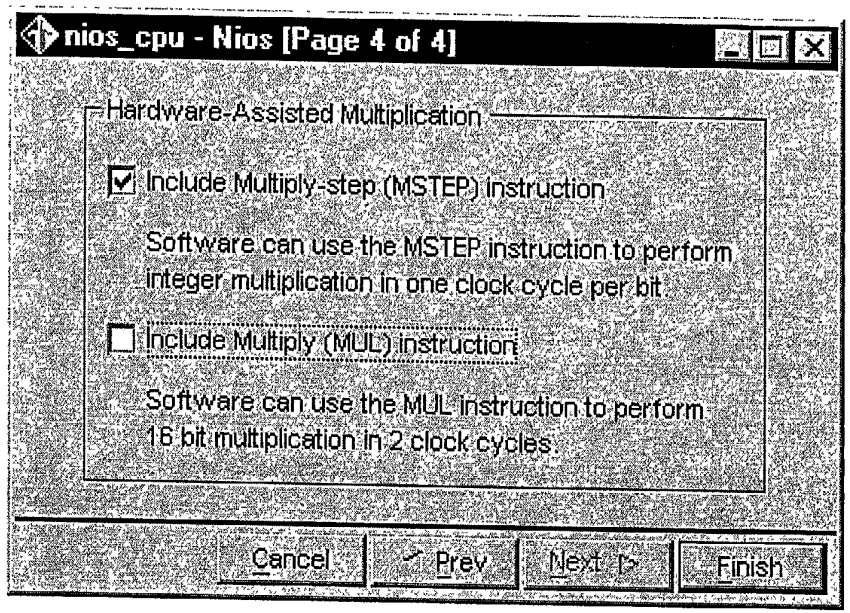

nios_cpu - Nios [Page 4 of 4]
Hardware-Assisted Multiplication
Include Multiply-step (MSTEP) instruction
Software can use the MSTEP instruction to perform integer multiplication in one clock cycle per bit.
Include Multiply (MUL) instruction
Software can use the MUL instruction to perform 16 bit multiplication in 2 clock cycles.
Cancel
< Prev
Next >
Finish

FIGURE 3G

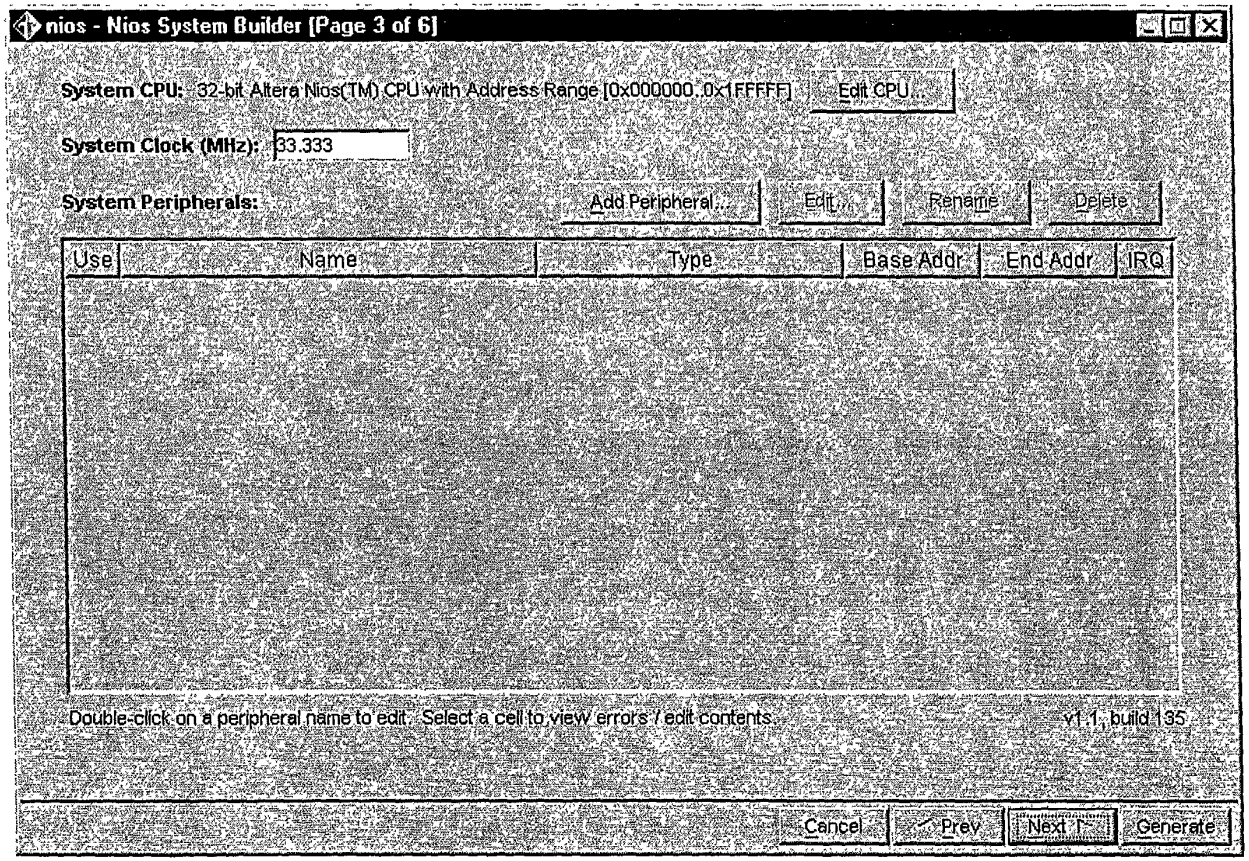


FIGURE 3H

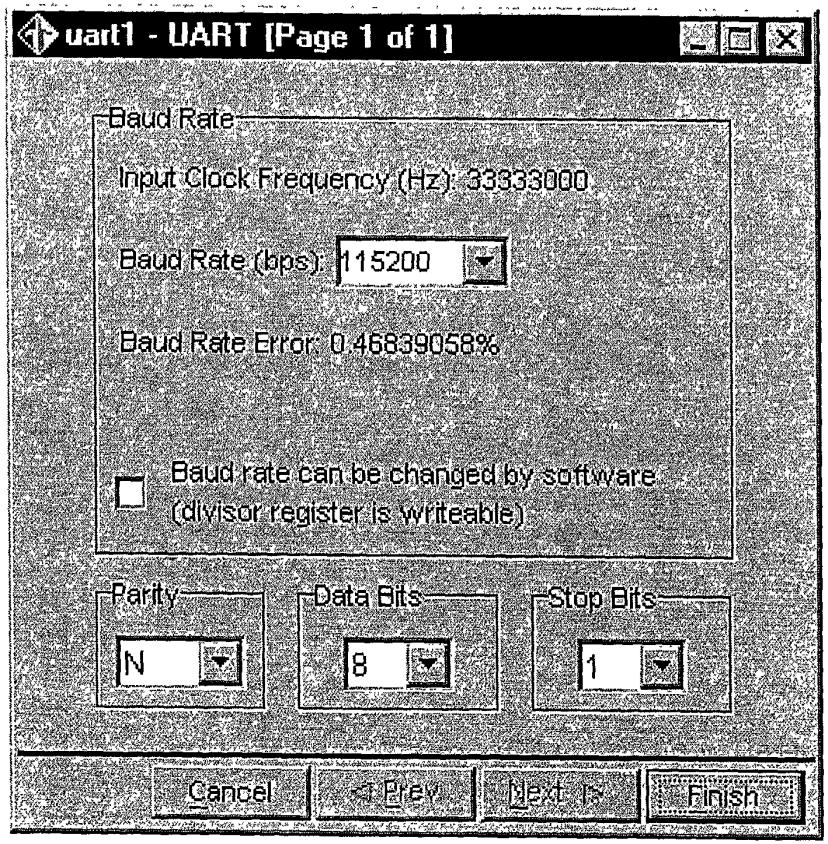

uart1 - UART [Page 1 of 1]
Baud Rate
Input Clock Frequency (Hz): 33333000
Baud Rate (bps): 115200
Baud Rate Error: 0.46839058%
Baud rate can be changed by software
(divisor register is writeable)
Parity
N
Data Bits
8
Stop Bits
1
Cancel
< Prev
Next >
Finish

FIGURE 3I

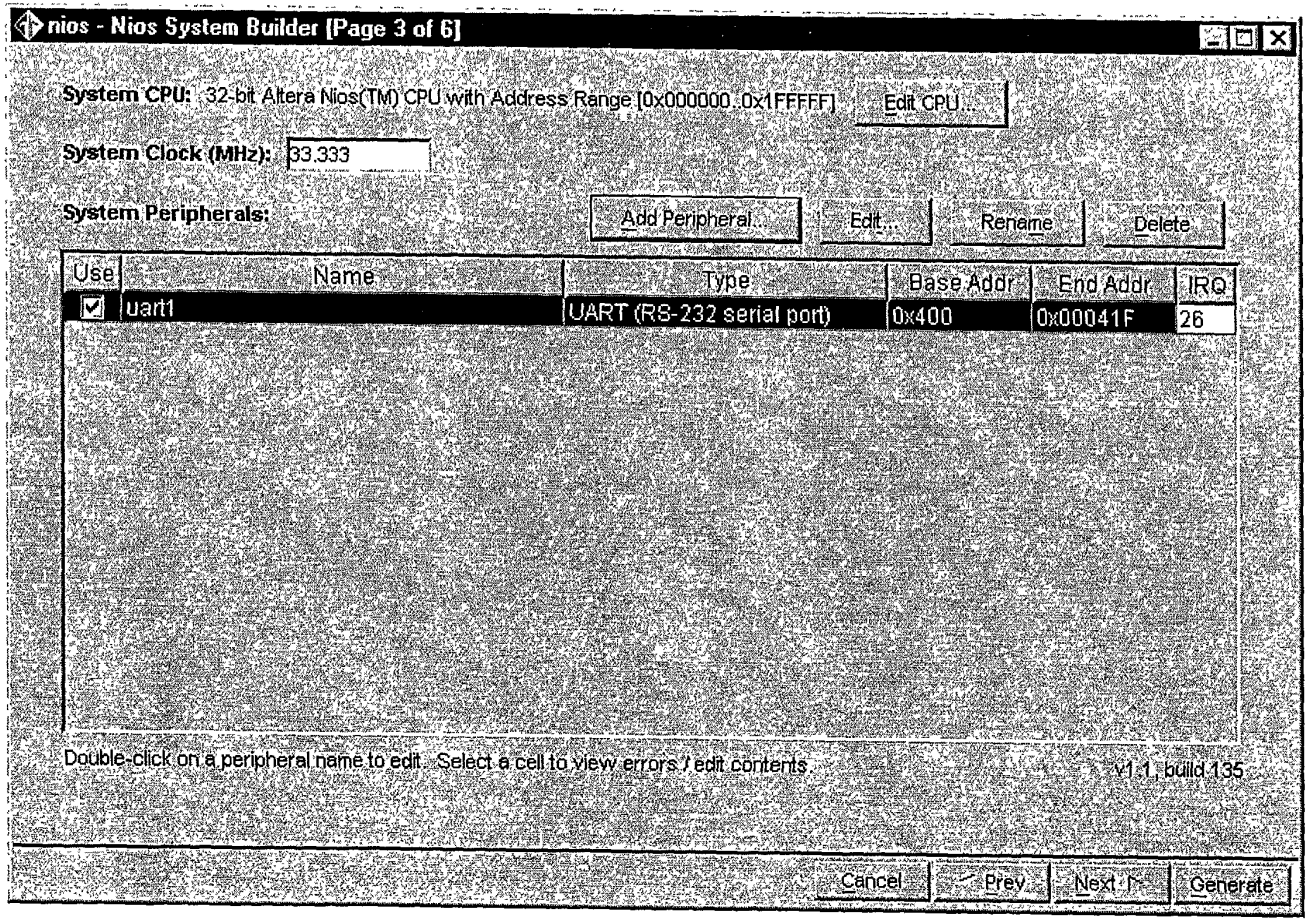


FIGURE 3J

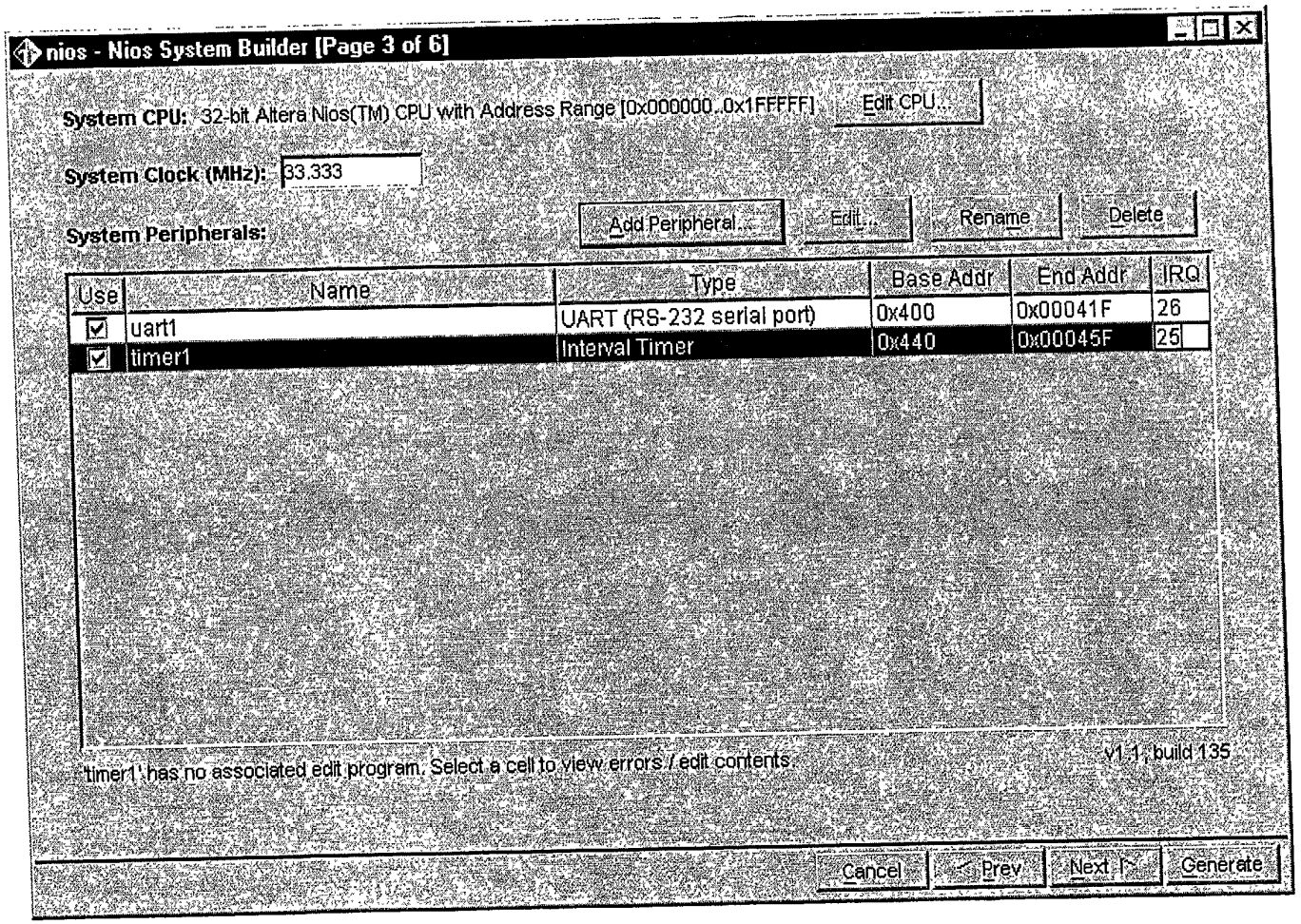

nios - Nios System Builder [Page 3 of 6]
System CPU: 32-bit Altera Nios(TM) CPU with Address Range [0x000000..0x1FFFFF]
Edit CPU...
System Clock (MHz): 33.333
System Peripherals:
Add Peripheral...
Edit...
Rename
Delete
Use
Name
Type
Base Addr
End Addr
IRQ
uart1
UART (RS-232 serial port)
0x400
0x00041F
26
timer1
Interval Timer
0x440
0x00045F
25
'timer1' has no associated edit program. Select a cell to view errors / edit contents
v1.1 build 135
Cancel
< Prev
Next >
Generate

FIGURE 3K

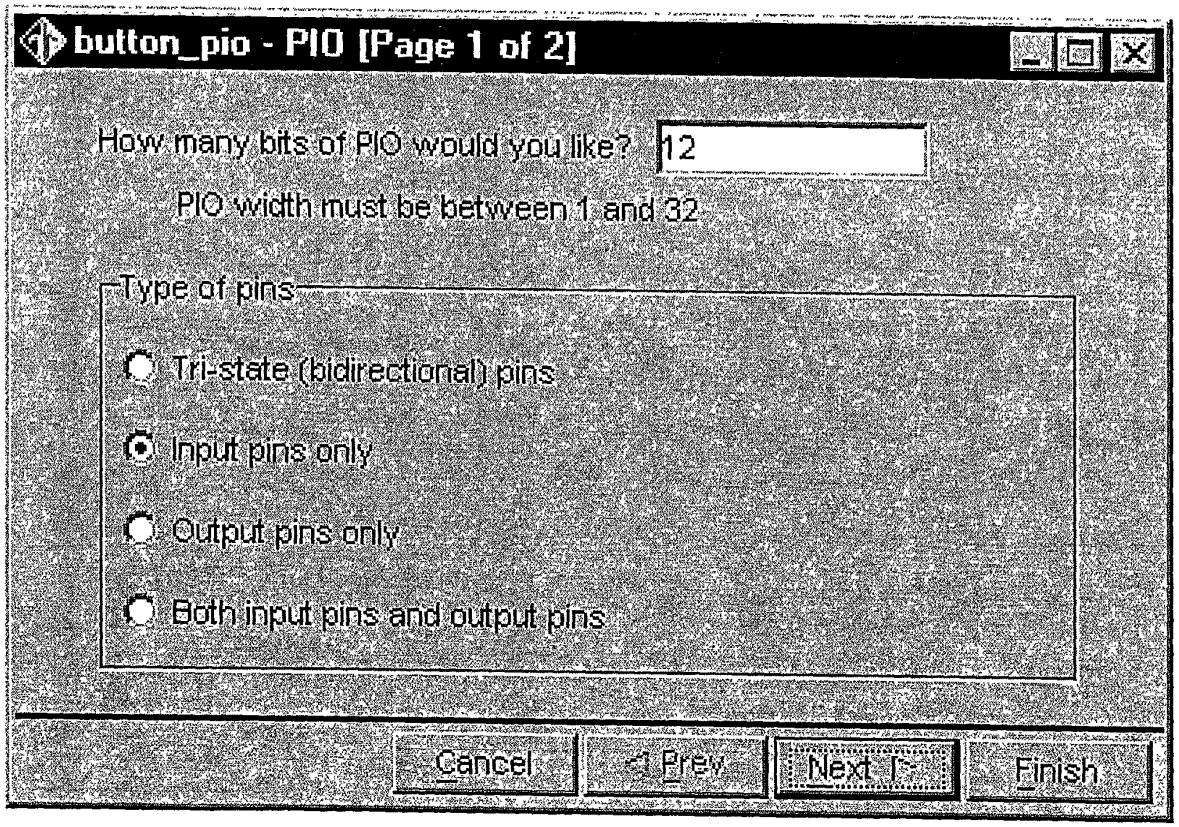


FIGURE 3L

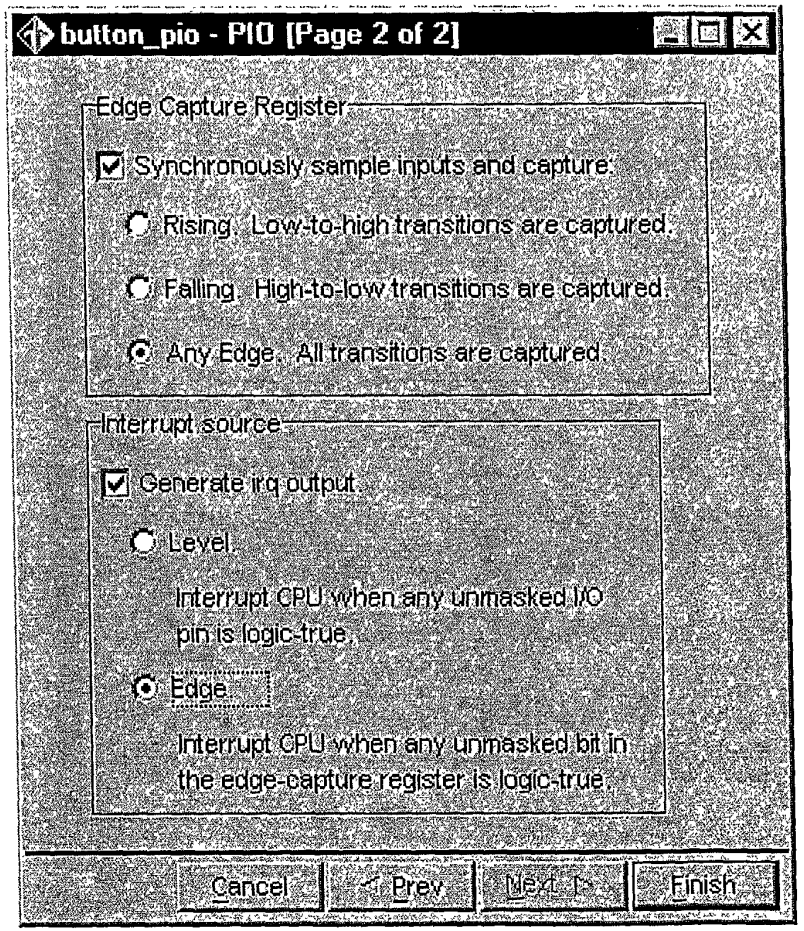


FIGURE 3M

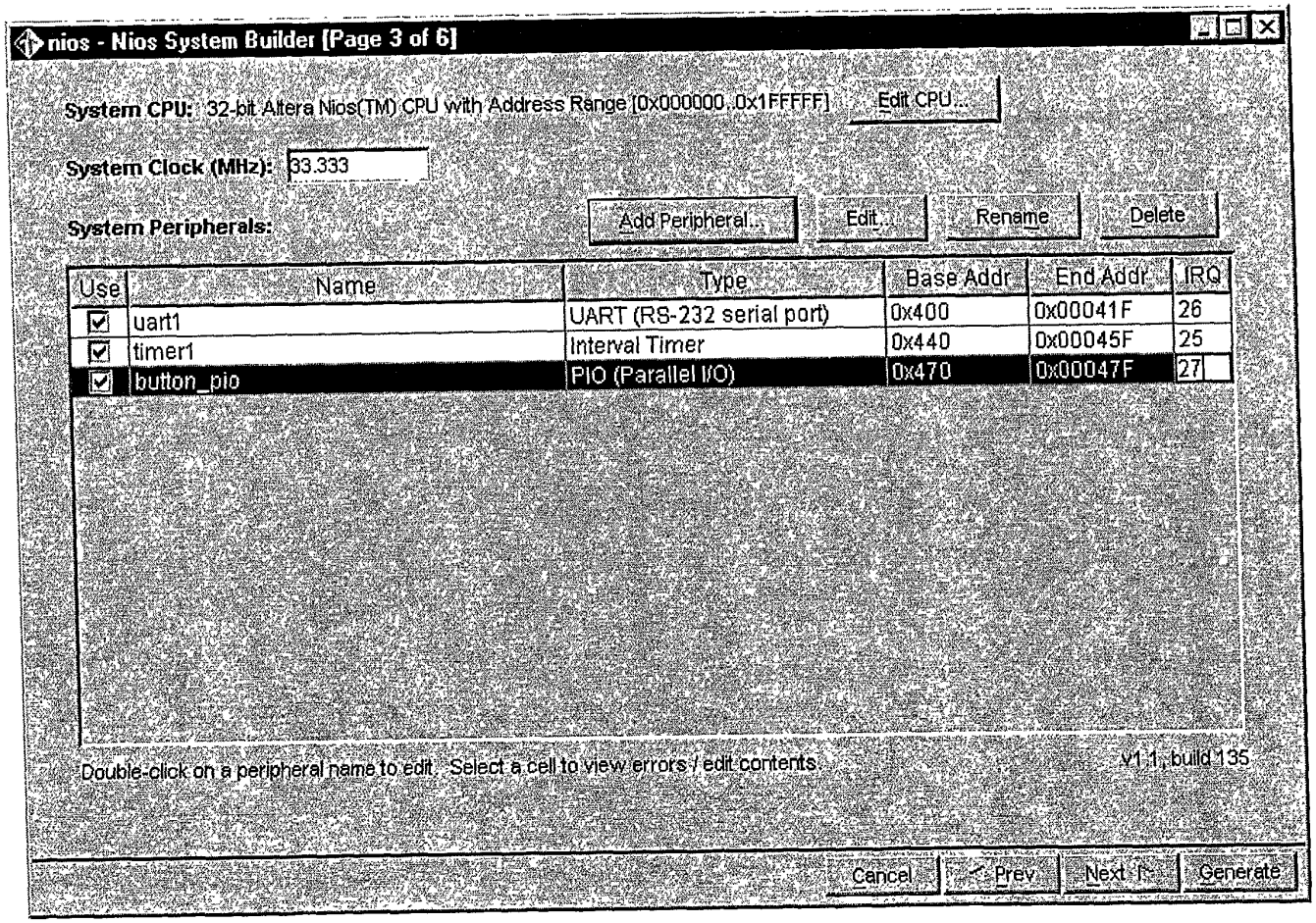

nios - Nios System Builder [Page 3 of 6]
System CPU: 32-bit Altera Nios(TM) CPU with Address Range [0x000000..0x1FFFFF]
Edit CPU...
System Clock (MHz): 33.333
System Peripherals:
Add Peripheral...
Edit...
Rename
Delete
Use
Name
Type
Base Addr
End Addr
IRQ
uart1
UART (RS-232 serial port)
0x400
0x00041F
26
timer1
Interval Timer
0x440
0x00045F
25
button_pio
PIO (Parallel I/O)
0x470
0x00047F
27
Double-click on a peripheral name to edit. Select a cell to view errors / edit contents.
v1.1 build 135
Cancel
< Prev
Next >
Generate

FIGURE 3N

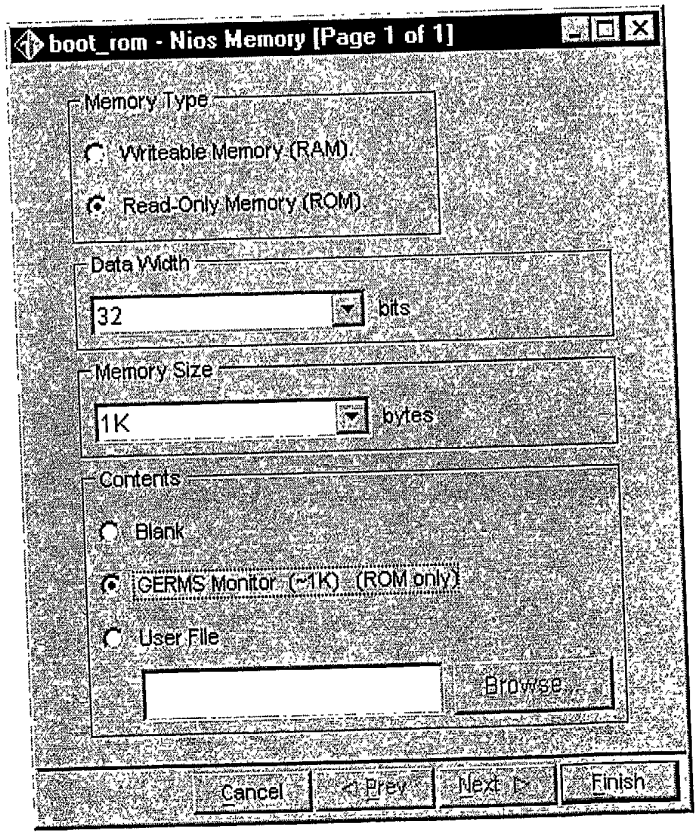
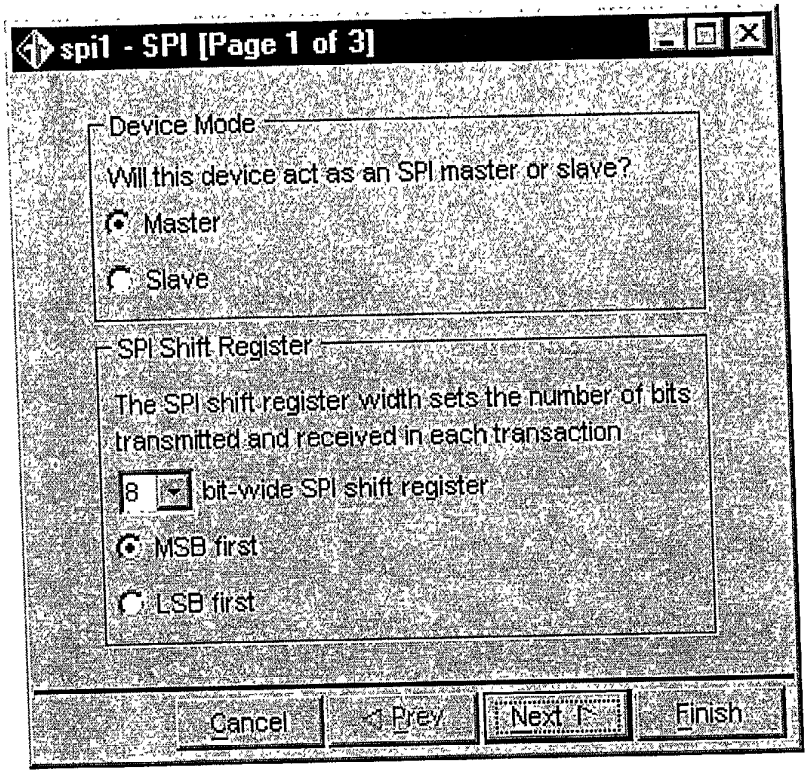


FIGURE 30


spi1 - SPI [Page 1 of 3]
Device Mode
Will this device act as an SPI master or slave?
Master
Slave
SPI Shift Register
The SPI shift register width sets the number of bits transmitted and received in each transaction
8
bit-wide SPI shift register
MSB first
LSB first
Cancel
< Prev
Next >
Finish

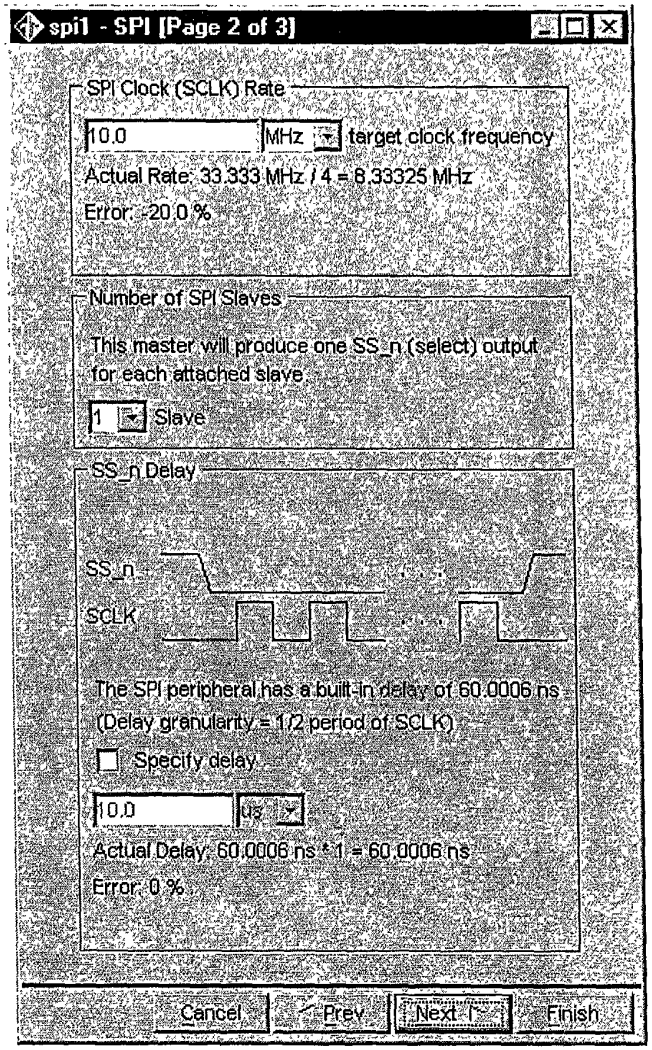


FIGURE 3P

FIGURE 3Q

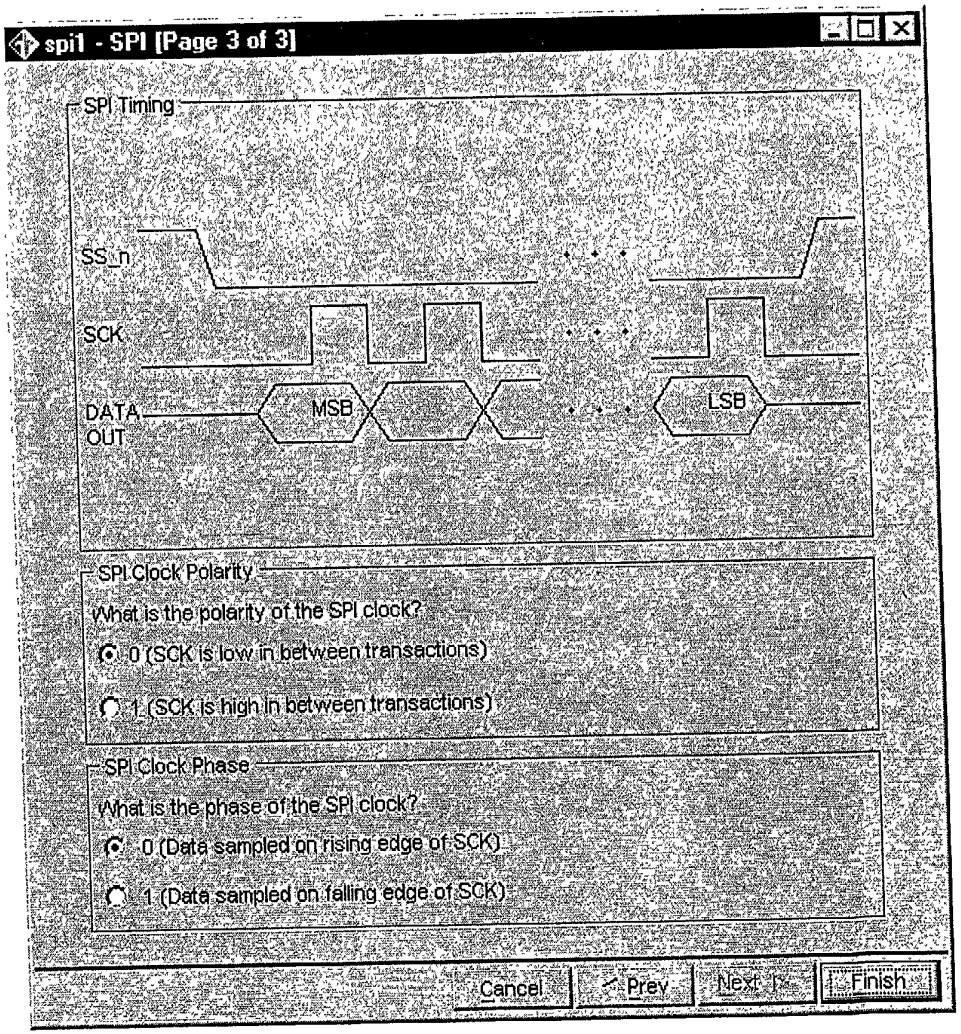

spi1 - SPI [Page 3 of 3]
SPI Timing
SS_n
SCK
DATA OUT
MSB
LSB
SPI Clock Polarity
What is the polarity of the SPI clock?
0 (SCK is low in between transactions)
1 (SCK is high in between transactions)
SPI Clock Phase
What is the phase of the SPI clock?
0 (Data sampled on rising edge of SCK)
1 (Data sampled on falling edge of SCK)
Cancel
< Prev
Next >
Finish

FIGURE 3R

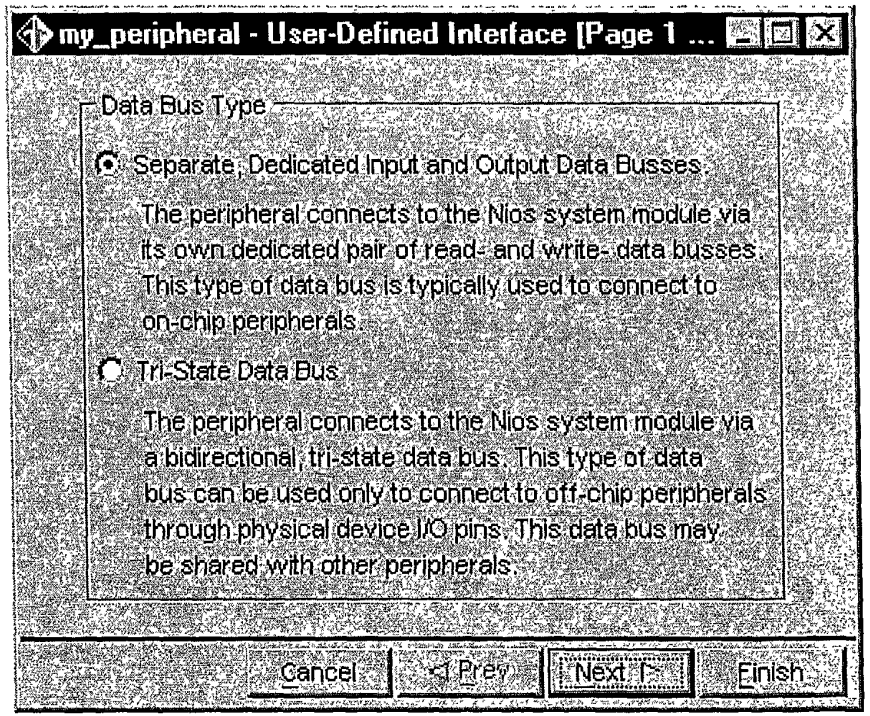


FIGURE 3S

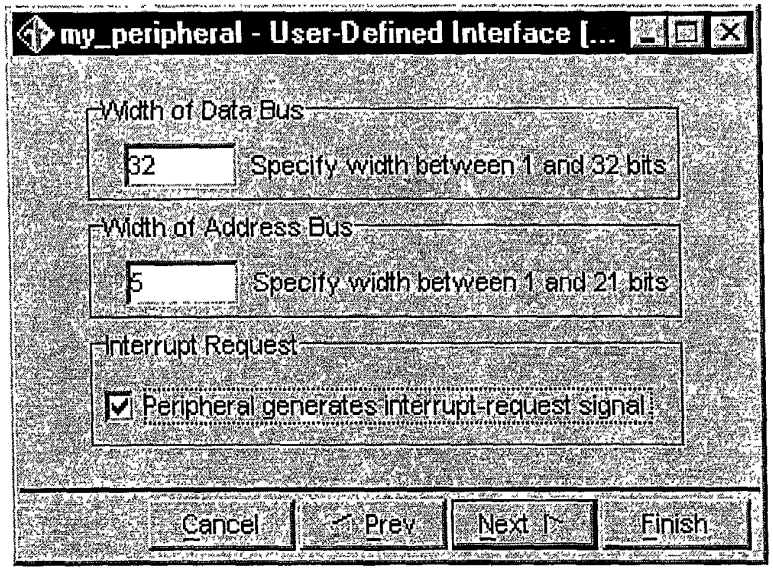


FIGURE 3T

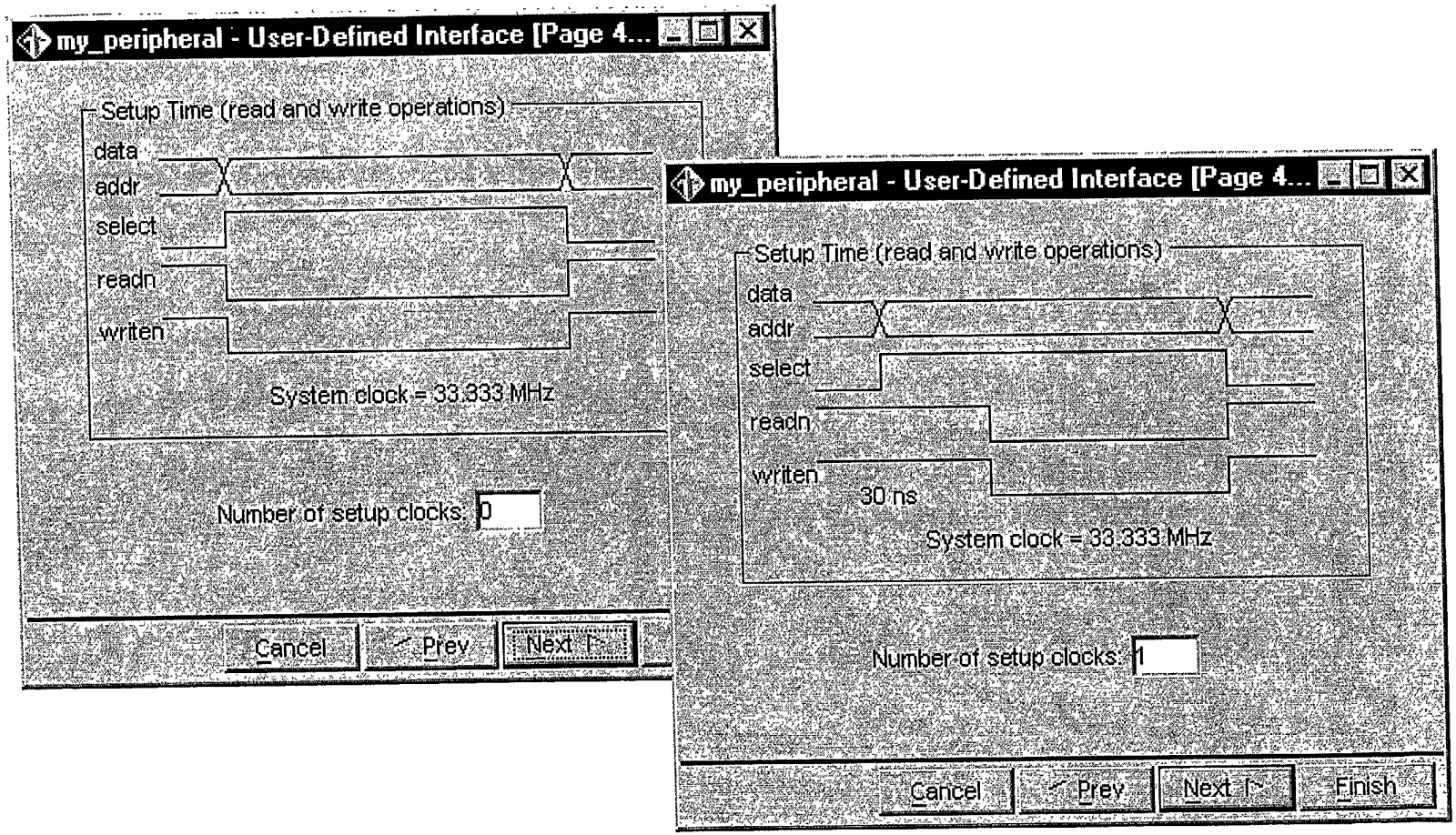


FIGURE 3U

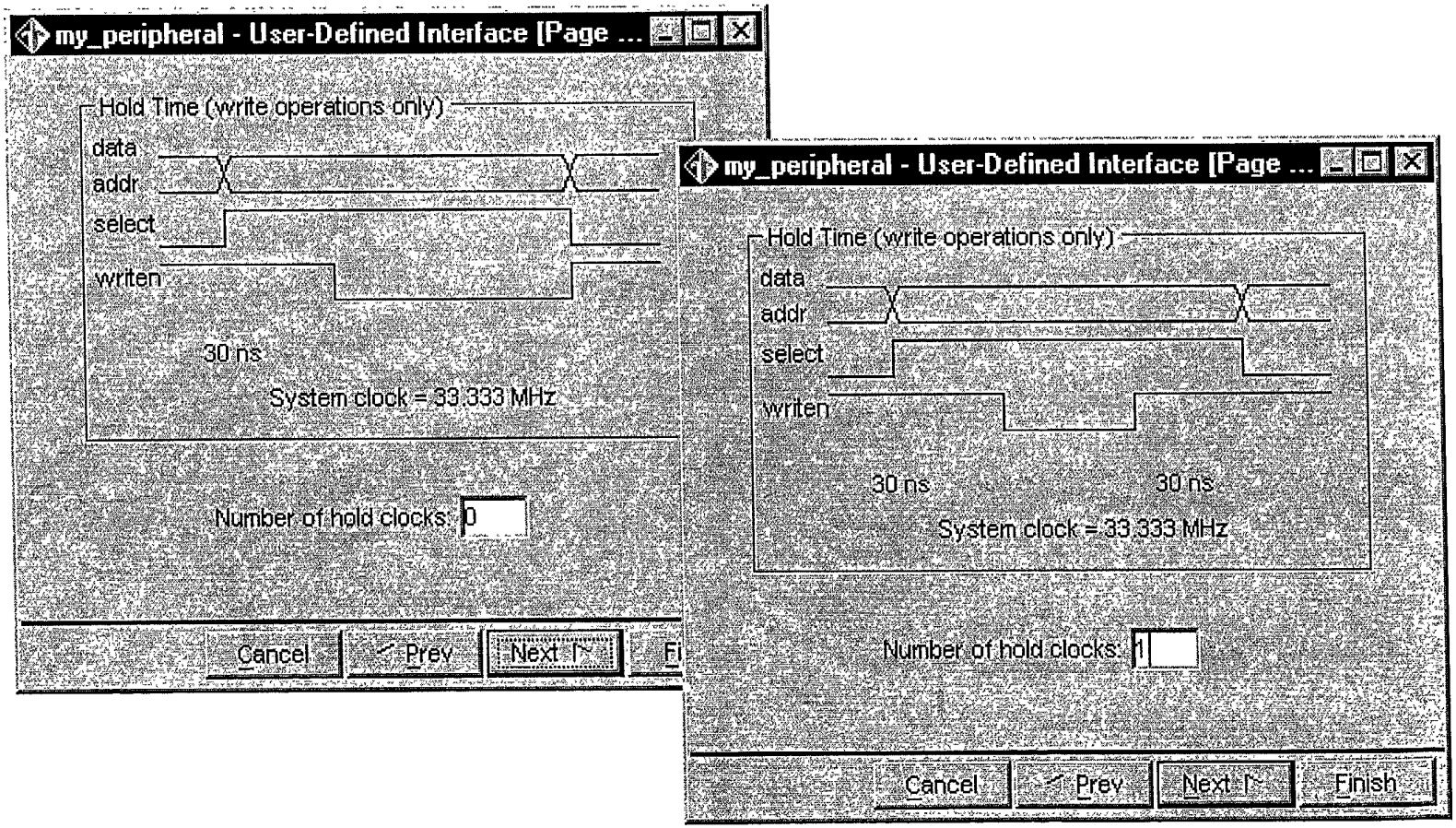

my_peripheral - User-Defined Interface [Page ...
Hold Time (write operations only)
data
addr
select
writen
30 ns
System clock = 33.333 MHz
Number of hold clocks: 0
Cancel
< Prev
Next >
Fi
my_peripheral - User-Defined Interface [Page ...
Hold Time (write operations only)
data
addr
select
writen
30 ns
30 ns
System clock = 33.333 MHz
Number of hold clocks: 1
Cancel
< Prev
Next >
Finish

Figure 3V

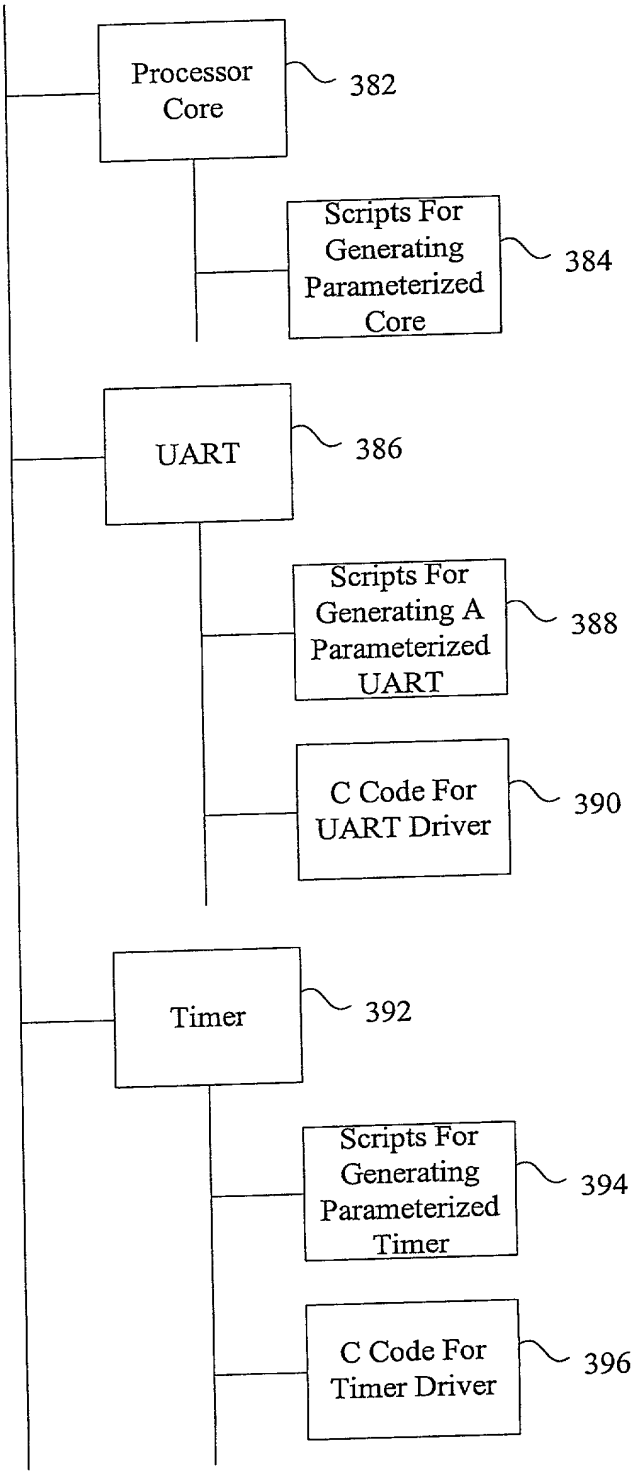

Processor Core
382
Scripts For Generating Parameterized Core
384
UART
386
Scripts For Generating A Parameterized UART
388
C Code For UART Driver
390
Timer
392
Scripts For Generating Parameterized Timer
394
C Code For Timer Driver
396

Figure 4

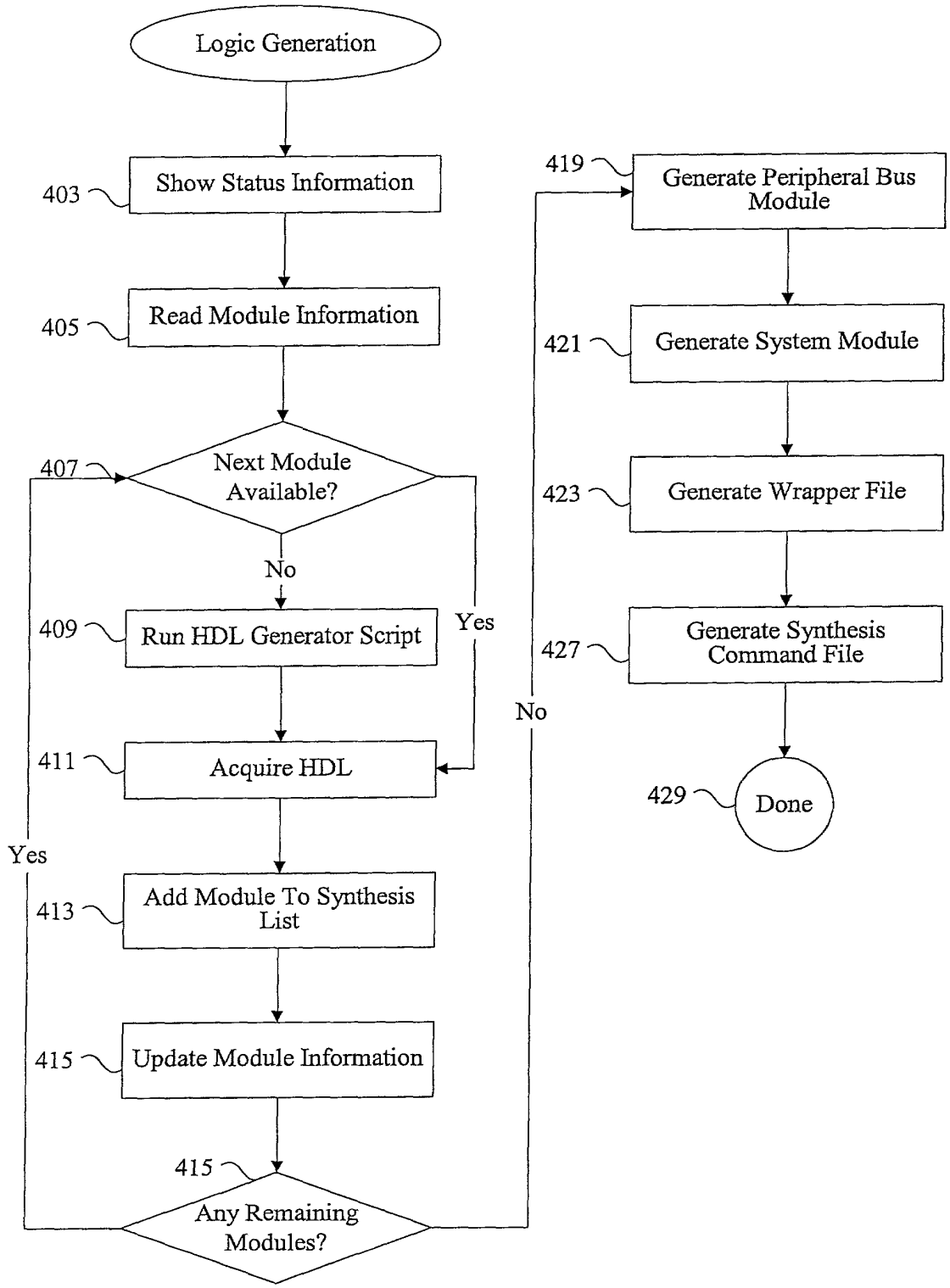

Logic Generation
403
Show Status Information
405
Read Module Information
407
Next Module Available?
No
Yes
409
Run HDL Generator Script
411
Acquire HDL
Yes
413
Add Module To Synthesis List
415
Update Module Information
415
Any Remaining Modules?
No
419
Generate Peripheral Bus Module
421
Generate System Module
423
Generate Wrapper File
427
Generate Synthesis Command File
429
Done

Figure 5

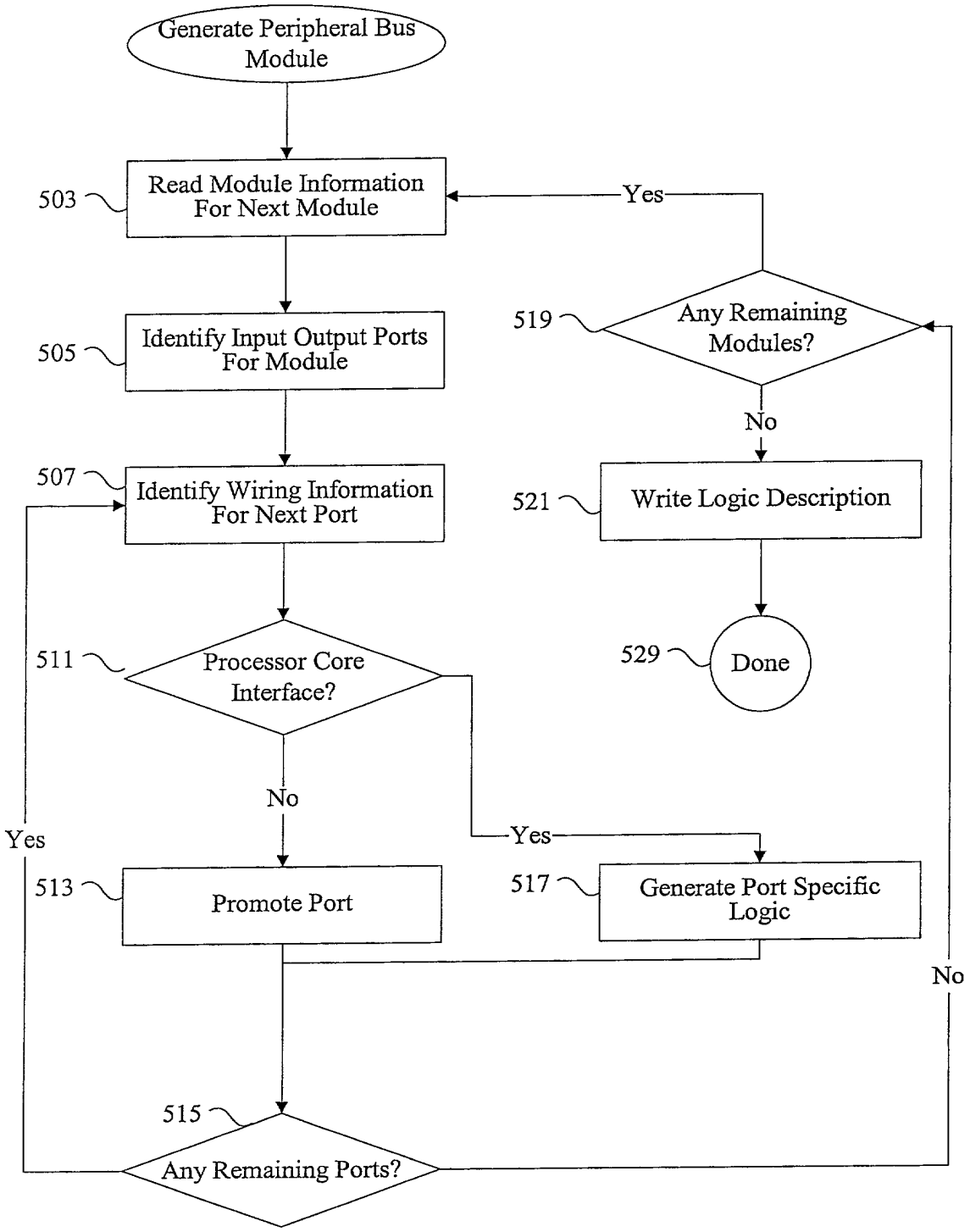

Generate Peripheral Bus Module
503
Read Module Information For Next Module
505
Identify Input Output Ports For Module
507
Identify Wiring Information For Next Port
511
Processor Core Interface?
No
Yes
513
Promote Port
Yes
517
Generate Port Specific Logic
515
Any Remaining Ports?
Yes
519
Any Remaining Modules?
No
521
Write Logic Description
529
Done
No

Figure 6A

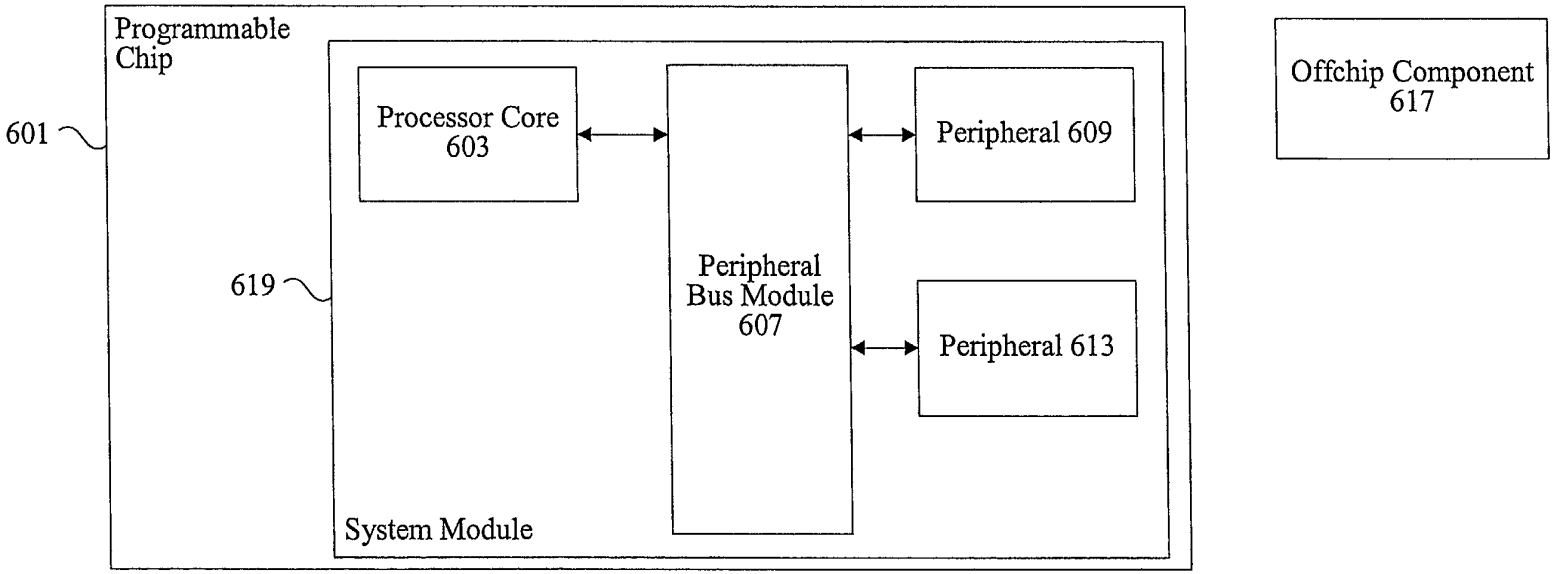

Programmable Chip
601
619
Processor Core 603
Peripheral Bus Module 607
Peripheral 609
Peripheral 613
System Module
Offchip Component 617

Figure 6B

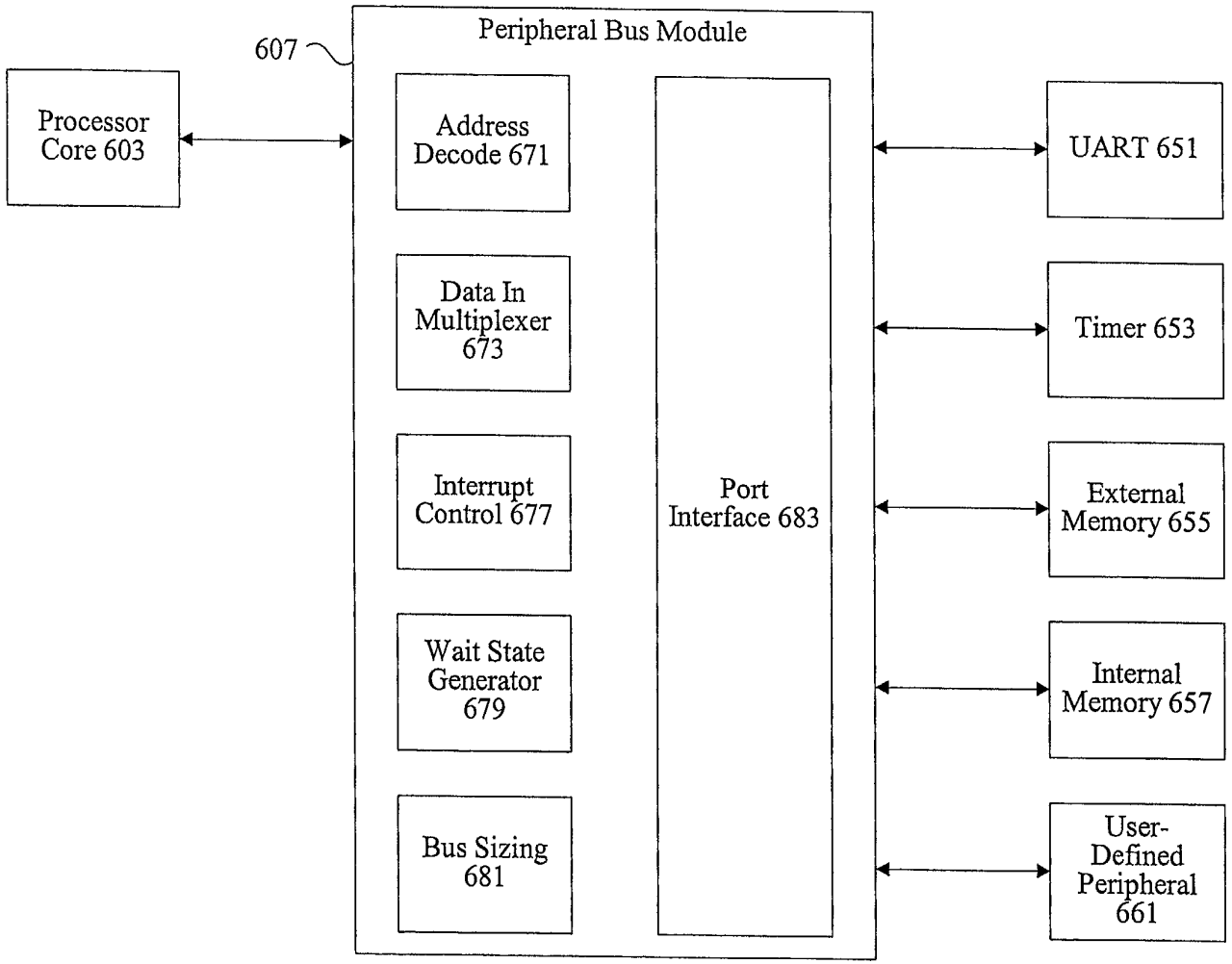

Peripheral Bus Module
607
Processor Core 603
Address Decode 671
Data In Multiplexer 673
Interrupt Control 677
Wait State Generator 679
Bus Sizing 681
Port Interface 683
UART 651
Timer 653
External Memory 655
Internal Memory 657
User-Defined Peripheral 661

FIGURE 7

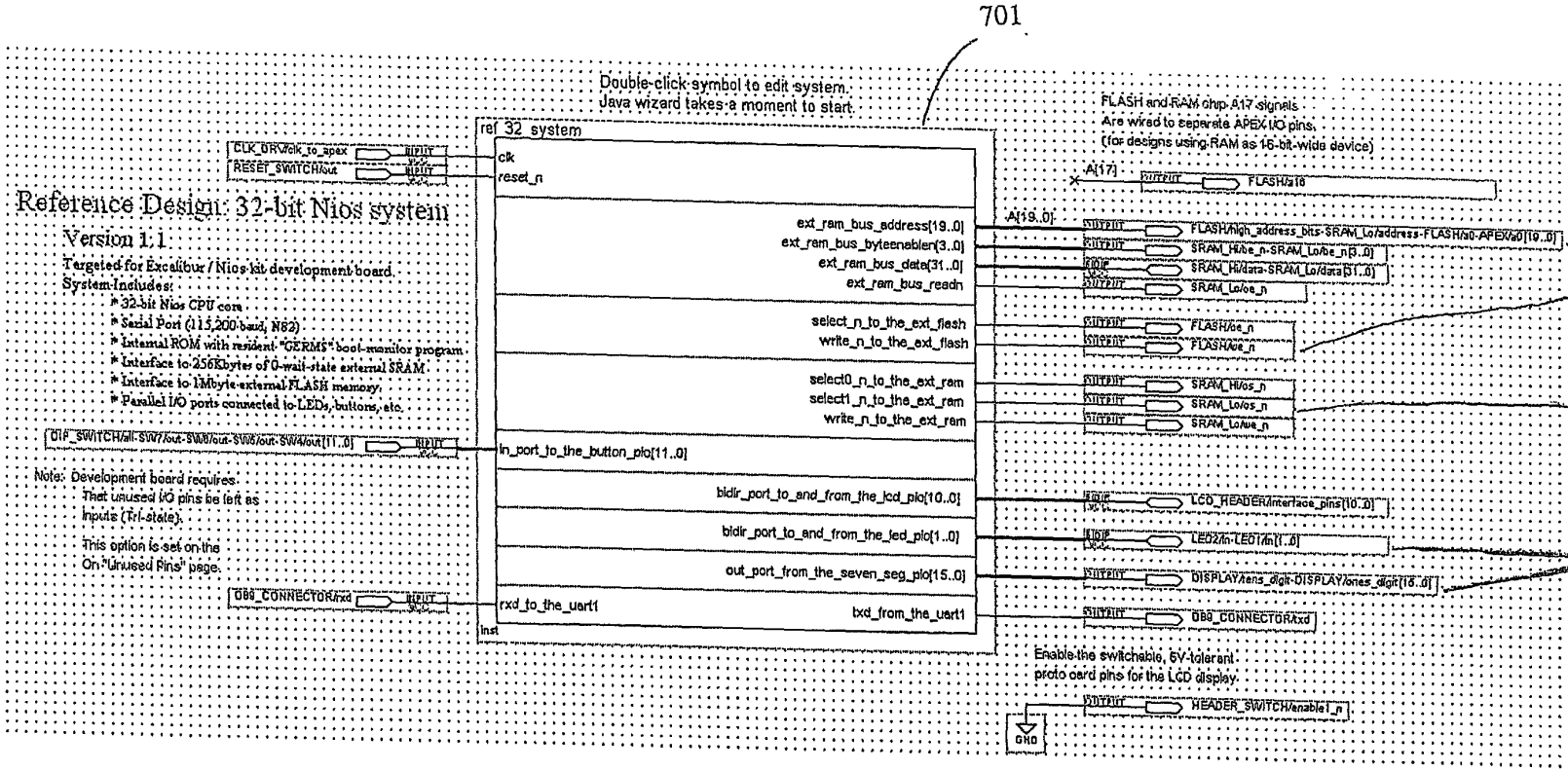
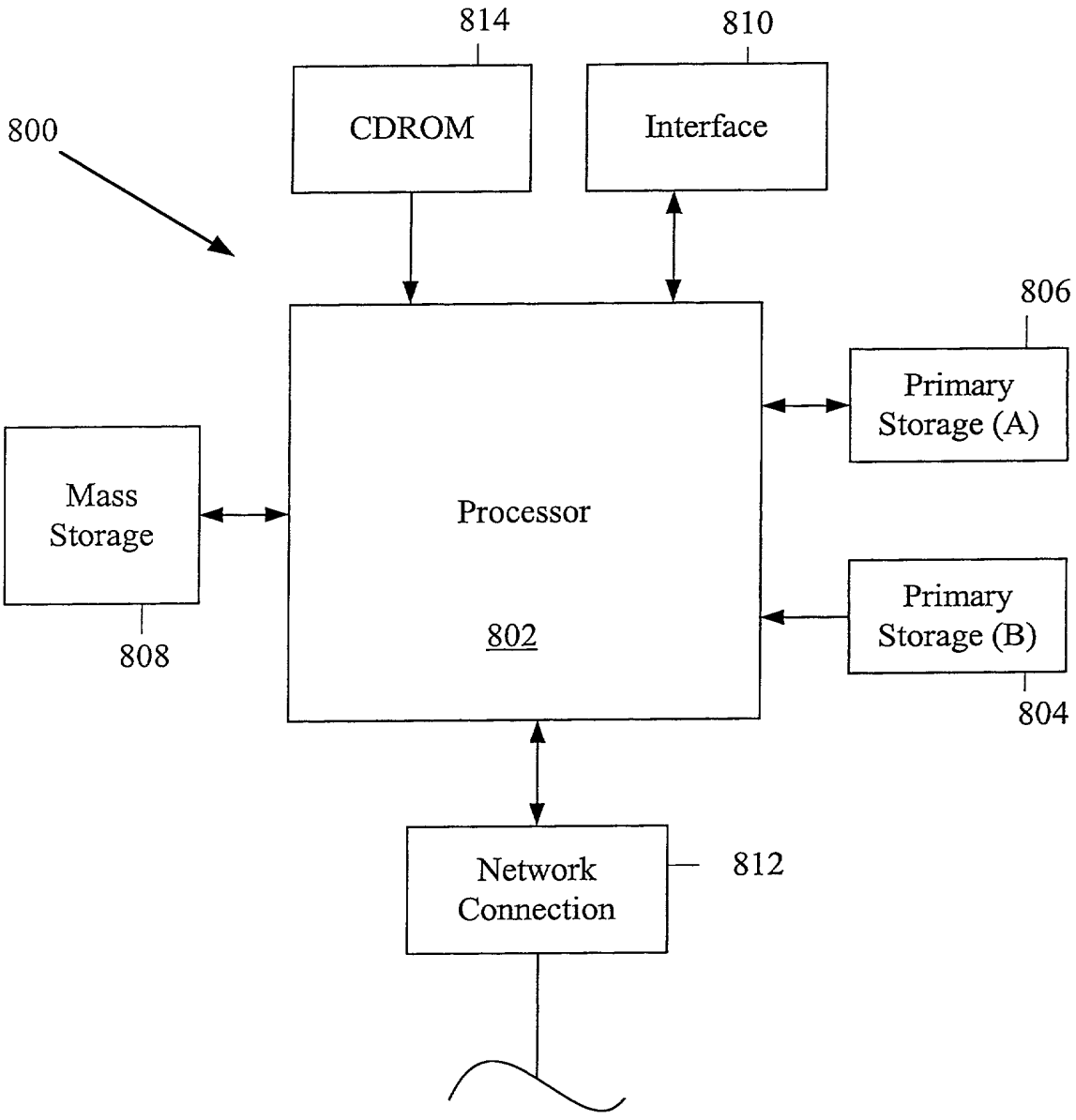

701
Double-click symbol to edit system.
Java wizard takes a moment to start.
ref 32_system
Reference Design: 32-bit Nios system
Version 1.1
Targeted for Excalibur / Nios kit development board.
System Includes:
* 32-bit Nios CPU core
* Serial Port (115,200 baud, N82)
* Internal ROM with resident "GERMS" boot-monitor program
* Interface to 256Kbytes of 0-wait-state external SRAM
* Interface to 1Mbyte external FLASH memory
* Parallel I/O ports connected to LEDs, buttons, etc.
Note: Development board requires
That unused I/O pins be left as
inputs (Tri-state).
This option is set on the
On "Unused Pins" page.
CLK_OR/clk_to_apex
RESET_SWITCH/out
DIP_SWITCH/all-SW7/out-SW8/out-SW5/out-SW4/out[11..0]
DB9_CONNECTOR/rxd
clk
reset_n
ext_ram_bus_address[19..0]
ext_ram_bus_byteenablen[3..0]
ext_ram_bus_data[31..0]
ext_ram_bus_readn
select_n_to_the_ext_flash
write_n_to_the_ext_flash
select0_n_to_the_ext_ram
select1_n_to_the_ext_ram
write_n_to_the_ext_ram
in_port_to_the_button_pio[11..0]
bidir_port_to_and_from_the_lcd_pio[10..0]
bidir_port_to_and_from_the_led_pio[1..0]
out_port_from_the_seven_seg_pio[15..0]
rxd_to_the_uart1
txd_from_the_uart1
inst
FLASH and RAM chip A17 signals
Are wired to separate APEX I/O pins.
(for designs using RAM as 16-bit-wide device)
A[17]
A[19..0]
FLASH/a16
FLASH/high_address_bits-SRAM_Lo/address-FLASH/a0-APEX/a0[19..0]
SRAM_Hi/be_n-SRAM_Lo/be_n[3..0]
SRAM_Hi/data-SRAM_Lo/data[31..0]
SRAM_Lo/oe_n
FLASH/oe_n
FLASH/we_n
SRAM_Hi/cs_n
SRAM_Lo/cs_n
SRAM_Lo/we_n
LCD_HEADER/interface_pins[10..0]
LED/n-LED1/n[1..0]
DISPLAY/tens_digit-DISPLAY/ones_digit[15..0]
DB9_CONNECTOR/txd
Enable the switchable, 5V-tolerant
proto card pins for the LCD display.
HEADER_SWITCH/enable1_n
GND
705
707
713

Figure 8


814
810
CDROM
Interface
800
806
Primary Storage (A)
Mass Storage
Processor
802
Primary Storage (B)
808
804
Network Connection
812